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(57) Abstract

A multilayer wiring board may be manufactured by a process which uses a sinterable conductive composition to fill via holes. The sinterable composition sinters reactively and/or non-reactively during the lamination cure cycle of the wiring board. Additional non-conductive components of the composition are described that may be included to offer structural, fluxing and other benefits.

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METALLURGICALLY BONDED POLYMER VIAS

TECHNICAL FIELD OF THE INVENTION

This invention pertains to methods of manufacturing printed wiring boards generally, and more specifically to a method of forming electrically conductive vias in laminates.

BACKGROUND ART

Multilayer wiring boards for the purposes of this disclosure are defined as electrical interconnection structures having more than two electrically conductive relatively planar layers separated from each other by dielectric. The electrically conductive layers of the wiring board may be electrically interconnected at discrete locations through electrically conductive vias. The vias extend perpendicular to and between electrically conductive planes, and therefore extend through dielectric layers.

Multilayer wiring boards are of great importance in the electronics industry where space is at a premium. In addition, the multilayer technology serves the needs for high speed circuits and for highly complicated circuit routing, where there are many crossings of wiring. While an equivalent circuit might be formed from a double sided single dielectric layer circuit board, the single layer board will require many times the space. Because of the extra length and width required, single layer boards may be mechanically or structurally deficient for many applications. Further, the long signal traces in single layer boards create electrical deficiencies which become more severe as operating frequencies increase. Small and fast multilayer circuits are therefore particularly desired in a number of applications.

Multilayer circuits are fabricated using a number of different techniques. The choice of particular materials and techniques generally depends upon price and reliability required for the application. For very high reliability applications such as military and medical devices, multilayer circuits are commonly formed from glass and ceramic tapes and noble metal

conductive compositions. These circuits are exceptionally stable, both mechanically and environmentally. The glass and ceramic substrates and noble metals have proven resistant to a large number of otherwise corrosive liquids and vapors while offering structural integrity and low thermal expansion.

Manufacturing multilayer substrates from glass and ceramic requires a very high temperature process referred to as sintering. For the purposes of this disclosure, sintering is defined as the diffusion and resulting agglomeration of particles that occurs at temperatures below the melting point of at least some of the particles. The sintering process converts an organic polymer bound glass frit and ceramic powder composite into the solid glass and ceramic composite of final form, free of polymer.

During the initial heating step of the sintering process, polymer binder is vaporized, oxidized or otherwise combusted. The remaining glass frit, noble metals and ceramic particles are then heated to an even higher temperature at which the glass softens and the ceramic and metal particles sinter together to form larger particles and eventually complete structures. Within these structures, the sintered conductor patterns yield electrically interconnected wiring patterns.

The temperatures required to remove polymer binder and sinter ceramic particles are very high, making the processing steps difficult and costly. Noble metal conductive materials are expensive, and the processing required to make glass and ceramic tapes of sufficient quality is also very costly. In summary, in spite of the many performance advantages offered by ceramic tapes and precious metal conductives, multilayer wiring boards manufactured using this process are in many applications simply too expensive.

A lower cost alternative which has found wide spread application is an organic polymer multilayer wiring board. In this construction, layers or sheets of polymer dielectric material are patterned with conductive wiring. One common form of this structure is a copper clad, glass reinforced epoxy board.

The copper will typically be bonded in foil or sheet form directly to a sheet of the polymer. The resultant laminate may then be cured completely, or merely have any solvents removed in a process commonly referred to as B-staging. Holes through the dielectric polymer layers are punched or drilled, and then these holes are made electrically conductive through an electrolytic or electroless plating process. Several of these laminates may then be assembled and bonded in a final lamination step, or, as is more preferred in the prior art, the layers may be built up in sequential fashion.

In the case of B-staged layers, the materials themselves may provide adequate flow and cross-linking to produce a stable structure after lamination. Where the dielectric layers are fully cured prior to final lamination, intervening layers of adhesives are used. The adhesive layers are placed between the fully cured layers and then the structure is laminated.

While the organic multilayer wiring board uses less costly materials and manufacturing processes, the resulting structure is also less reliable than a ceramic counterpart. During lamination, the organic material is prone to flowing in somewhat unpredictable ways. This flow may damage relatively fragile vias, particularly where these vias are only very thinly deposited copper. Further, in the case of a single step final lamination of multiple layers, there is a lack of reliable bonding structure between layers. In the case of a sequential build, any product which fails after several of the sequential steps will have a great deal of invested value lost. The sequential build will also subject the first laminate to a large number of cure and lamination cycles which further adversely affects yield.

Unfortunately, increasing the thickness of copper in the via may not be adequate to attain a desired yield. Copper and polymer typically have very different thermal coefficients which may lead to destructive failure. Both the lamination step and operation of the circuit thermally stress the board. Plating thicker copper reduces elasticity somewhat, increasing the probability of failure during thermal stress. Additionally, cost begins to escalate as more copper is deposited.

An alternative approach to plated copper as a via material is conductive polymer. Exemplary

of this approach are U.S. patents 4,967,314 and 5,117,069 by Higgins, which disclose a silver filled epoxy via fill material. Silver filled polymer vias offer great elasticity when compared to solid metal vias. Additionally, organic binders used within the via may be of the same composition or very similar composition as the board, yielding an excellent thermal expansion match.

In spite of the advantages, these prior art filled polymer vias are difficult to produce with low electrical resistance, high yield and good environmental stability. The polymer component in these prior art vias is not conductive. Instead, conductivity occurs as a result of points of contact between individual filler particles. Even silver filler particles are not perfectly corrosion and contamination resistant, and may further be sensitive to moisture and handling.

Point contact must also be established between the via filler particles and the planar conductive patterns of each layer. This point contact is adversely affected by thermally or mechanically induced physical motion. Poor point contact with the planar patterns results in increased electrical resistance through the via, just as if the via material itself had high electrical resistance. Point contact simply does not offer the electrical conductivity and reliability of solid metal conductors.

Because multilayer circuits are best applied to highly complex wiring patterns and high speed circuits, high or erratic via resistance is not acceptable. Manufacturing yields of complex circuits are severely impacted, and, since these circuits are the most expensive to manufacture, poor yields are very costly. High resistance vias also limit the available speed of operation, and, where particularly erratic, may result in very unreliable field performance of a finished circuit. Because of these limitations in electrical resistance, yield and environmental stability, filled polymer vias are only infrequently used in the manufacture of multilayer wiring boards.

Yet another prior art technique for manufacturing multilayer organic wiring boards involves an additive technique. In this process a non-conductive, typically polymeric substrate is selectively coated with a conductive material. The conductive material contains a relatively low melting point metal or alloy powder, a relatively high melting metal powder, and an

adhesive flux mixture.

The coated substrate is warmed to evaporate a solvent and then heated rapidly to the melting point of the low melting metal or alloy. Subsequently, the substrate is heated at the cure temperature of the adhesive flux. Post cure heating may also be necessary to achieve complete cure and optimal adhesion, depending upon requirements.

During curing of the adhesive flux of the conductive material, conductive constituents sinter to form a very reliable metallurgical bond. The sintering process used is a transient liquid phase sintering process, which is defined herein as a process of melting a mixture of two or more different powders to the melting point of one of the powders, followed by consumption of the liquid phase through diffusion alloying with a still solid higher melting powder. The resulting sintered structure is solid even at the melting temperature of the low melting particulate.

Perhaps the most widely known example of transient liquid phase reactive sintering is the formation of a dental amalgam. Mercury, a liquid at room temperature, is mixed with finely divided silver or other similar metal to form an alloy. Once formed, the dental alloy resists temperatures well above room temperature.

In order to form a multilayer wiring board from the above described single layer board, a dielectric layer is applied over the cured and sintered conductive material. The dielectric material is patterned to form via holes or passages, cured, and a second layer of conductive material is selectively applied. The second layer of conductive material will then be cured similarly to the cure of the first conductive layer. The process of applying and curing conductive and dielectric material may be repeated multiple times to create a multilayer wiring board, with vias formed by conductive material filling via holes in the dielectric. Holes may be drilled or punched in the resulting multilayer structure, and the inside walls of the holes coated with the conductive material to produce conductive through holes.

The resulting multilayer wiring boards exhibit excellent conductivity and environmental

stability. Formation of a sintered conductive structure provides little opportunity for conductivity deterioration due to oxidation, corrosion or thermal expansion and contraction.

However, the formation of vias using this prior art technique is unreliable. Gases are prone to entrapment within a dielectric passage, between an already formed and cured conductive layer and the freshly deposited via material. Voids and bubbles, as noted hereinabove, are not acceptable in the manufacture of complex multilayer wiring boards.

Further, punched, laser drilled or chemically etched vias may be manufactured to much smaller size than a screen printed via. The structures which result from this additive process may not be as dense as desired, due to the larger via size.

The sequential processing required to manufacture additively additionally results in a large number of large thermal cycles during manufacture. Any product which fails after several of the sequential steps will have a great deal of invested value lost. The sequential build will also subject the first laminate to a large number of cure and lamination cycles which further adversely affects yield.

DISCLOSURE OF INVENTION

In accord with the present invention, a method of manufacturing a polymer dielectric multilayer wiring board includes forming conductive patterns and vias from an organic laminate stock material, filling the vias with a metallurgically bondable conductive material, stacking patterned and filled laminates together as individual laminae in a resulting laminate, and heating and pressing the laminate to permanently bond the laminae together and simultaneously metallurgically bond the via fill material.

A conductive sinterable composition useful in the practice of the method can include components that sinter, together with fluxing components and structural components. The composition is designed to sinter and cure within the temperature range of lamination.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 illustrates a cross-section of a first via produced in accord with the preferred embodiment of the invention.

Figures 2 and 3 illustrate by cross-section a second via produced in accord with the preferred embodiment of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the preferred embodiment a multilayer circuit with interconnection in the axis perpendicular to the circuit layers is achieved by filling vias prior to lamination. The via fill is a composite material that during lamination forms metallurgical bonds to itself and to the metal traces of the circuit.

The multilayer structure can be built up from either single sided circuits comprising a conductive layer and a dielectric layer or double sided circuits comprising a dielectric layer between two conductive layers. Double sided circuits typically have metallized through holes connecting one conductive layer to the other. When using double sided circuits, a bond ply is used between double sided circuits. The bond ply consists of an adhesive dielectric material, most commonly with filled vias. When using single layer circuits, vias are typically formed (by any suitable means, such as drilling, punching, laser drilling or etching) in the circuit after an adhesive is applied to the dielectric side of the circuit.

Possible dielectrics include those known in the prior art manufacture of additively or subtractively formed circuitry. The dielectrics are preferably thin, unfilled and dimensionally stable. They are even more preferably amenable to continuous reel-to-reel processing, as used by some manufacturers of flex circuits. Preferred materials include Upilex™ and Kapton E™ copolymer polyimides.

Adhesives can be liquid or dry film, thermoplastic or thermoset, and filled or unfilled. The adhesive is preferably expansion matched to copper and the dielectric.

In accord with the invention, a conductive constituent of the via fill material forms intrinsic metallurgical bonds and also metallurgically bonds to any metal circuit traces or metallized via sidewalls that it contacts. The metallurgical bond is superior to point contact conduction achieved with conventional filled polymer materials and may be accomplished several ways.

One simple alternative embodiment for metallurgical bonding involves wetting by and subsequent intermetallic formation with a low melting point metal or alloy. "Low melting" is understood in this context to mean below the temperatures that are expected to be encountered during lamination. An example of this approach is the use of a tin lead or other solder alloy paste as the via fill material.

The paste consists of finely divided solder alloy, a suitable flux, and a vehicle consisting of a volatile solvent and small quantities of rheological additives. Using this approach, vias can be filled in the individual circuit layers by screen printing, stenciling or other techniques. Heat is then applied, either in a single lamination/via "curing" step or in a 2-step heat treat and laminate operation. In either case, during lamination at least some portion of the solder particles melt, wet, and form a metallurgical bond with each other and any circuit or via side wall metal present, typically copper.

Unfortunately, the volatile solvent content of solder paste creates a via with a significant volume fraction of voids. The voids reduce the reliability of contact to adjacent vias. Additionally, solvent removal during lamination can be a problem.

An alternative embodiment soldering method that overcomes this objection is depositing solder particles within each via that are substantially the same dimension as the vias prior to lamination or cure. Solder balls are commercially available and many systems exist for mechanically placing them in controlled position to high accuracy. Ink jet technology also can be used to project molten solder into controlled positions.

Regardless of the deposition method, the completed structure using these alternative embodiment fill compositions has thermal and mechanical properties related to the properties of the solder used. Typically, creep strength and fatigue properties are limited. In soldering, interfacial intermetallics may form but the bulk of the bond is comprised of the bulk solder alloy. Solders will therefore remelt at the temperature used to form the metallurgical bond. This may limit subsequent packaging operations such as die attach, etc.

Examples of low melting alloys are listed in Table 1:

TABLE 1.

ALLOY	°C
Sn Ga	20
In Ga	16
Ga Zn	25
Ga	30
Sn Pb Bi In Cd	46.5
Sn Pb Bi In	58
Sn Bi In	61
Sn Pb Bi Cd	70
Bi In	72.4
Sn Bi In	79
Pb Bi Cd	91.5
Sn In Cd	91
Sn Pb Bi	95
Sn Bi Cd	103
Sn In	117
Pb Bi	125
In Cd	127
Sn Bi	139
Bi Cd	144

Sn Pb Cd	145
In	157
Sn Tl	170
Sn Cd	176
Sn Pb Ag	178
Sn Zn	198
Pb Au	215
Sn Ag	221
Sn	232
Pb Cd	248
Pb Sb	251
Cd Zn	266
Bi	271
Au Sn	280
Pb As	288
Pb Ag	304
Pb Zn	318
Cd	321
Au Ge	356
Au Si	370

A more preferred bonding method involves reactive sintering. For the purposes of this disclosure, reactive sintering is defined as a sintering process where compound formation within inter-particle bonds consumes one or more components of the original mixture. For example, copper may be bonded with tin using reactive sintering. All of the tin originally present as a liquid is consumed in the formation of higher melting point copper tin intermetallic bonds that bind individual copper particles to each other. The thermal and mechanical properties of the intermetallic are very different from the starting tin material. Such a bond, substantially all of which consists of intermetallic, can be formed by solid state diffusion. However, raising the temperature above the melting point of one of the constituents greatly accelerates the diffusion

process. To lower the temperature at which this rapid diffusion occurs, one of the intermetallic forming elements (tin, in this case) can be alloyed with one or more materials that will form a lower melting phase. Examples may be found in Table 1. In this case, the final metallurgical bond would consist of copper tin intermetallics plus the residual alloying element.

Another alternative embodiment metallurgical bond is formed by applying heat and or pressure to a metal powder. Surface energy driven surface diffusion results in material transport to the points of particulate contact, resulting in the growth of a neck of material connecting the two particles. Metal to metal bonding without the formation of a compound (intermetallic or otherwise) at the bond neck is defined for the purposes of this disclosure as non-reactive sintering. Non-reactive solid state sintering requires temperatures on the order of one-half the absolute melting point of the materials involved to proceed at a suitable rate.

The sintering temperature can be reduced substantially by the presence of a liquid phase due to enhanced diffusion. Critical factors to consider are: the ability of the liquid phase to wet the solid, the ability of the liquid to form intermetallics with the solid phase (which may cause a shift towards reactive sintering), the solubility of the solid in the liquid phase and the liquid in the solid phase and the ratio of the solid-solid and solid-liquid surface energies.

The preferred embodiment via fill materials illustrated by example below exhibit sintering including both reactive sintering and non-reactive sintering. The resulting combination of intermetallic and same metal bonds gives the sintered via a combined performance which includes intermetallic characteristic and unalloyed characteristic. Conductive materials in accord with the preferred embodiment generally contain components belonging to each of four categories.

The first component is a relatively high melting particulate phase material. By high melting, we mean that the material remains solid at the highest processing or anticipated use temperature of the circuit. The material must be wet by the liquid phase material described below and must be capable of at least one of the following:

a. Sintering to itself and the circuit metallization at or below expected lamination

temperatures; and/or

b. Forming an intermetallic compound with one or more components of the liquid phase.

Suitable materials include copper, nickel, gold and silver, though copper is thought to be the most preferred material.

The second component category material forms a liquid phase at temperatures below expected lamination temperatures. The liquid must at least partially wet the first component high melting material. Exemplary materials of this category include metals and alloys from Table 1. Tin/lead alloys are used in the preferred embodiment. 60/40 tin/lead in conjunction with copper solid phase is an example of a system where intermetallic/intermetallic and copper/copper bonds may both be expected to form. In other words, this is an example of both reactive and non-reactive sintering.

The third component category material is a space-filling, mechanical property enhancing material that will occupy the interstices of the metal network of the thermally treated via fill material. This material may be used to provide resilience to the via structure, thereby lessening the probability of failure. It may be likened to the formation of a fine network not unlike multi-strand conductor. As is well known, multi-strand conductor offers greater flexibility than solid core wire.

The third component may also be used to design a more thermally matched via structure. Additionally, the resilience referred to may also provide for better tolerance of thermally induced stress.

This third component material is much preferred for structural reasons, but is not essential. Organic thermosetting and thermoplastic resins are two classes of materials that may be used. The presence of the uncured thermosetting resin in the unheated via fill paste contributes also to a rheology suitable for screen printing, though volatile solvents may similarly be used. If solvents are used, they must be removed prior to lamination, or, as noted with discussion of solder paste, destructive outgassing and voids may result.

Resole phenolics and epoxy based materials are preferred. Other preferred materials may be selected, provided they have cure kinetics such that they do not interfere mechanically or chemically with the metallurgical reactions between the solid/solid or solid/liquid phase until adequate bonds are formed. Preferred materials also provide fluxing action, or react with fluxing agents present as a separate class of materials, in such a way that no corrosive material remains in the thermally treated via fill. Resole phenolic resin with excess aldehyde is an example of such a system.

The fourth component category material is capable of promoting wetting between the first and second component category materials. This fourth component category material may be required for all but the most noble metal systems chosen. A separate flux may be desirable. Fluxes will generally be organic materials with amine, acid, aldehyde, or acid chloride functional groups. Mildly activated rosin and water white rosin have both been used effectively.

EXAMPLE 1

A transient liquid phase sinterable via fill material exhibiting both reactive and non-reactive sintering was produced as follows:

1.3 grams of flux was prepared from Alpha 611 RMA flux supplied at 37 percent in alcohol by staging at 82°C to remove 60 ± 1% of the volatile content. 7.8 grams (7.8 weight percent) of a 70% solids resole phenolic resin (Oxychem Methylon 75108™) were mixed with the 1.3 grams of flux. 30.3 grams of nominally 10 micron 63/37 tin/lead solder particles and 60.6 grams of -325 mesh spherical copper particles were dispersed in the resin flux mixture. The copper powder was first reduced in forming gas at approximately 315°C for one hour to insure cleanliness. Approximately 0.5 grams of benzyl alcohol was added to adjust the viscosity to a value suitable for screen printing.

The volume fraction of constituents may be adjusted across a reasonable range. The metal content of the via fill will generally be as high as possible, while still allowing the proper rheology for via filling. This will generally limit the total metal content of the via fill to less than

80 volume percent, and more typically to between 40 and 70 volume percent. The proportion of liquid to solid phase at the onset of melting of the low melting point constituent at the beginning of the thermal cycle can be as low as a few volume percent, or up to about 50 volume percent of the solid phase. Lower percent liquid phase is not effective in promoting sintering, while higher volume percents cannot be consumed by the metallurgical reaction. The organic phase can be present from 0 to 60 volume percent.

EXAMPLE 2

A 6-metal layer interconnect structure was fabricated from single sided circuit layers using a transient liquid phase via fill material from example 1 as follows. Single sided circuits were produced from copper foil adhesively bonded to polyimide film by standard subtractive etching techniques. The polyimide film was DuPont Kapton H™ and the adhesive was DuPont Pyralux™. The foil was rolled and annealed one ounce copper. The copper/adhesive/Kapton material was packaged under the trade name Pyralux LF-9120. Artwork corresponding to the circuit pattern desired on each of the 6 metal circuit layers was produced and used to expose the photoresist coated Pyralux LF material. The photoresist was developed and the exposed copper was etched using a ferric chloride based etchant. The photoresist was removed and a modified epoxy adhesive sheet was heat tacked to the dielectric side of the panel containing the etched circuits. The adhesive was 1 mil Courtalds Z-Flex™ supplied on 1 mil mylar release sheet. The individual circuit layers were excised from the panel and both 4 mil and 8 mil diameter vias were punched through lands in the copper traces using a numerically controlled punch. Punch to die clearances were closely controlled to produce vias of the highest quality. The circuit and via pattern were chosen to demonstrate stacked, blind and buried vias in the final structure. Each via punched circuit layer was then via filled with the transient liquid phase sinterable material from example 1, as follows. The circuit was placed on the vacuum nest of the screen printer, circuit side down. Using the via punched mylar as a contact mask and using screen printer parameters familiar to those skilled in the art, the vias were fill with the via fill paste. Conditions were selected to produce a slightly convex via fill pattern on the circuit side of the laminate. The mylar release sheet was removed from the dielectric side producing a slightly convex via fill on the dielectric side of the circuit.

The via filled laminates were then assembled into multilayered circuits with and without an intermediate via cure. The intermediate cure consists of a short term heat treatment above the melting point of the starting liquid phase composition. In this case, the heat treatment was 2 minutes at 200°C. Best results were obtained without the intermediate cure. The individual via filled circuit layers were stacked in a lamination fixture that ensures alignment of the individual layer vias. The lamination schedule consists of pressure cycling between 500 and 1000 psi at room temperature to de-air the laminate, followed by pressure reduction to 250 psi. The press platens are then heated to approximately 382°F over a period of 20-25 minutes. The system was held at temperature and pressure for 70 minutes and then cooled to room temperature over a period of 15 minutes while being held at lamination pressure. The completed structure contained blind, buried and stacked vias of both 4 mil and 8 mil diameter in larger lands. The stacked 4 mil vias had a resistance of less than 50 milliohms. Cross sections of the vias are shown in Figure 1 and illustrate both reactive and non-reactive sintering. The locations in the photograph labelled by the numeral 1 are copper bonds, while those labelled as 2 are intermetallic bonds.

EXAMPLE 3

A 4 metal layer structure was fabricated from double sided circuits with plated through holes using a transient liquid phase via fill as follows. The double sided circuits were produced by vacuum metallizing one side of a copolymer polyimide (Upilex) with a "seed" layer of chrome/copper, punching the via pattern, then vacuum metallizing the second side and the vias. Photoresist was laminated to both sides and developed in such a fashion as to expose the seed layer in areas where copper metal was desired. Copper was plated up electrolytically. When the desired thickness of copper was reached, the photoresist was stripped and the seed layer was flash etched. The resulting circuits were approximately 6"x 6" and contained approximately 1.6 mil lines separated by 1.8 mil spaces on the first side and a substantially continuous copper ground plane on the second side. More than two thousand five hundred 2.5 mil diameter metallized vias connected the two sides.

Structures containing four metal circuit layers with stacked vias were fabricated from pairs of the double sided circuits by interleaving bond plies between the double sided circuits. The bond

plies were fabricated by first laminating adhesive and a release sheet to both sides of Upilex film. The adhesive was Courtalds Z-Flex™ 1 mil thick on a release sheet of polyester (Mylar™). The same via pattern present in the double sided circuit flex was punched in the bond ply with an 8 mil punch. An eight mil, rather than a 2 or 4 mil punch was used simply for reasons of convenience. The same 8 mil via pattern was also punched in a 2 mil metal foil creating a metal stencil for via filling.

The bond ply and circuit layers were placed on the vacuum nest of a screen printer. The via pattern in the metal stencil was registered to the bond ply or circuit via pattern. Via fill material from example 1 was applied to the stencil and, using screen printing parameters familiar to those skilled in the art, a via paste was printed into the bond ply or circuit vias. Again, a slightly convex via surface on both sides of the bond ply or circuit is advantageous.

Three kinds of multilayer assemblies were fabricated. Via filled circuits were laminated with via filled bond plies to a metal stiffener to form the first assembly. Unfilled circuits were laminated with via filled bond plies without a stiffener to form the second assembly. Via filled circuits were laminated with via filled bond plies without a stiffener to form the third kind of assembly. In all cases, the lamination schedule consisted of pressure cycling the stack between 500 and 1,000 psi at room temperature to de-air the laminate followed by a pressure reduction to 250 psi. The press platens were then heated to 382°F over a period of 25 minutes. The system was held at temperature and pressure for 70 minutes and then cooled to room temperature over a period of 15 minutes, while being held at lamination pressure.

The completed laminates contain vias all of which have a resistance of less than 50 milliohms. Figure 2(a) shows that the vias were formed by both non-reactive and reactive sintering, as shown at 1 and 2 respectively, and figure 2(b) shows a view of the structure from lower magnification, where the via and circuit layers are visible.

While the foregoing details what is felt to be the preferred embodiment of the invention, no material limitations to the scope of the claimed invention is intended. Further, features and design alternatives that would be obvious to one of ordinary skill in the art are considered to be

incorporated herein. The scope of the invention is set forth and particularly described in the claims hereinbelow.

CLAIMS

We claim:

1. A method of manufacturing an organic dielectric multilayer wiring structure comprising the steps of:

patterning electrical interconnect pathways upon a first organic containing stock material, thereby forming a patterned stock material;

forming via holes through a second organic containing stock material;

filling said vias with a sinterable and curable conductive composition, thereby forming a via filled stock material;

stacking said patterned stock material and said via filled stock material together to build an organic laminate, and

laminating at a first pressure and a first temperature to permanently bond said patterned stock material and said via filled stock material into said organic laminate and simultaneously sinter and cure said sinterable and curable conductive composition.

2. The method of claim 1 wherein said first temperature is greater than an ordinary room ambient.

3. The method of claim 1 wherein said first pressure is greater than an ordinary room ambient.

4. The method of claim 1 wherein said bonding further comprises cross-linking of said first or said second organic containing stock material.

5. The method of claim 1 wherein said first and said second organic containing stock material is a polymer film.

6. The method of claim 1 wherein said sintering occurs between said filled via and said electrical interconnect pathways and also within said filled via.

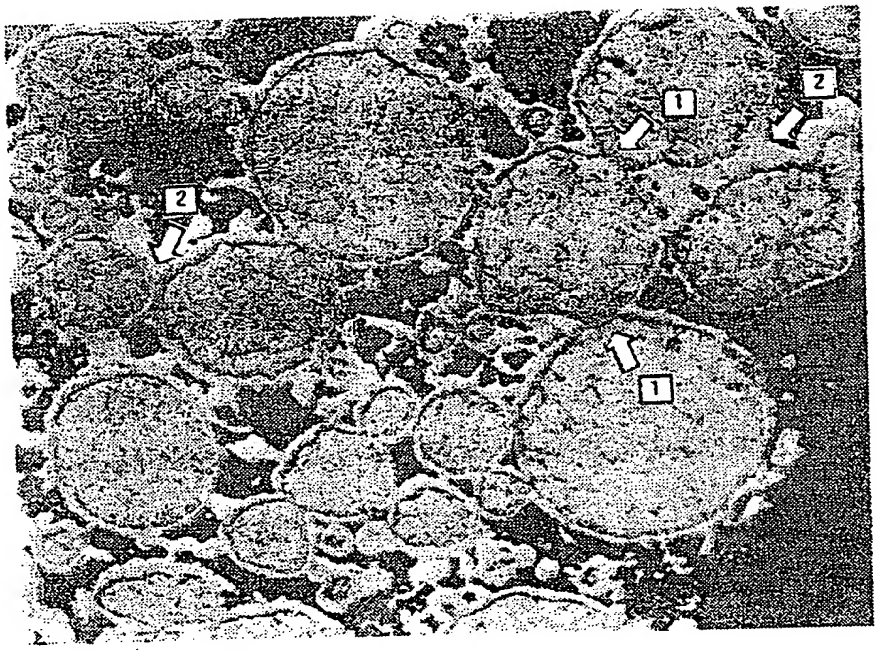


Figure 1

1) Copper/Copper Bond

2) Intermetallic/Intermetallic Bond

1000x

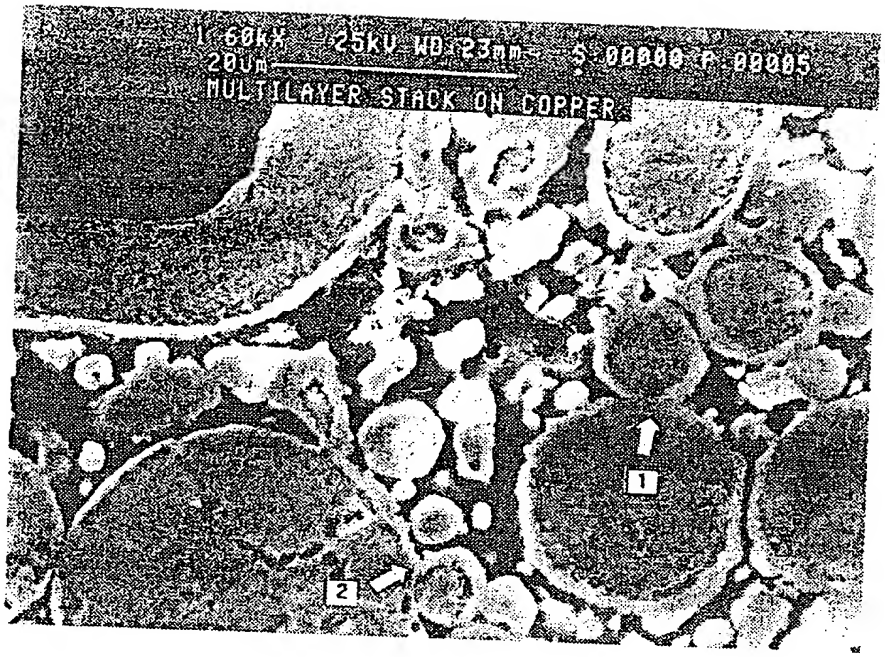
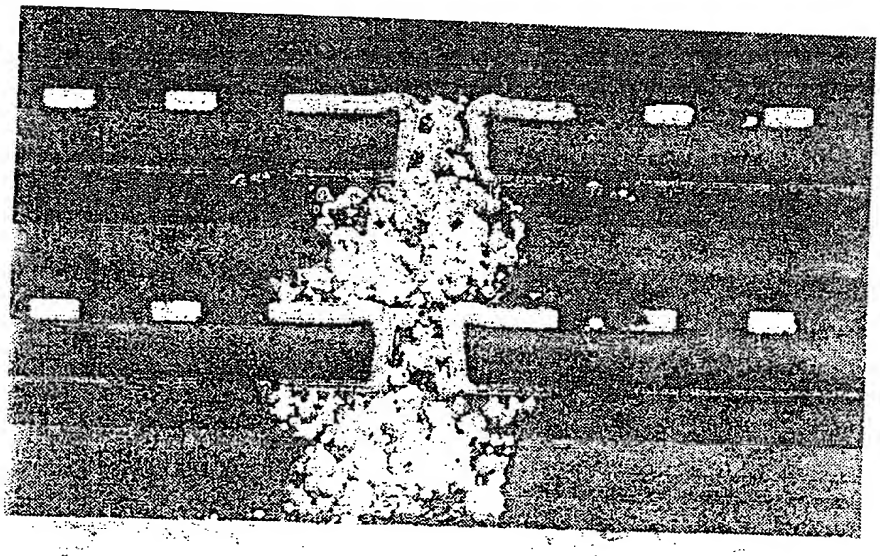


Figure 2A (1600X)

1) Copper / Copper Bond
2) Intermetallic / Intermetallic Bond



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/13361

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :B23K 35/34
US CL :148/24
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. :

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 3,077,511 (BOHRER ET AL) 12 February, 1963. See entire document.	1-6
A	US,A, 3,184,830 (LANE ET AL) 25 May 1965. See entire document.	1-6
A	US,A, 3,187,846 (POWELL) 08 June 1965. See entire document.	1-6
A	US,A, 3,202,879 (STERLING) 24 August 1965. See entire document.	1-6
A	US,A, 3,311,966 (SHAHEEN ET AL) 04 April 1967. See entire document.	1-6
A	US,A, 3,335,489 (GRANT) 15 August 1967. See entire document.	1-6

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
13 MARCH 1995

Date of mailing of the international search report
10 APR 1995

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/13361

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 3,340,600 (HARRIS) 12 September 1967. See entire document.	1-6
A	US,A, 4,679,122 (BELKE, JR., ET AL) 07 July 1987. See entire document.	
A	US,A, 4,874,721 (KIMURA ET AL) 17 October 1989. See entire doucment.	1-6
A	US,A, 4884,170 (OHKI ET AL) 28 November 1989. See entire document.	1-6
A	US,A, 4,902,857 (CRANSTON ET AL) 20 February 1990. See entire document.	1-6
A	US,A, 4,919,970 (HOEBENER ET AL) 24 April 1990. See entire document.	1-6
A	US,A, 5,062,896 (HUANG ET AL) 05 November 1991. See entire document.	1-6
A	US,A, 5,117,069 (HIGGINS, III) 26 May 1992. See entire document.	1-6
A	US,A, 5,128,746 (PENNISI ET AL) 07 July 1992. See entire document.	1-6
A	US,A, 5,147,084 (BEHUN ET AL) 15 September 1992. See entire document.	1-6
A,P	US,A, 5,280,414 (DAVIS ET AL) 18 January 1994. See entire document.	1-6